Track Total Credits: 20 (6-8-6)
Domain Code : VLCU2070

Courses Division:

- ASIC Design (2-1-0)
- Digital VLSI (2-2-0)
- Analog VLSI (2-1-0)
- VERIFICATION USING SYSTEM VERILOG & UVM (0-4-0)
- Project (0-0-6)

Code	Course Title	T-P-Pj (Credit)	Prerequisite
VLCU2070	ASIC Design	2-1-0	NIL

Objective

- The objective of the course is to provide understanding of the entire logic design process with the analysis from combinational and sequential digital circuit design.
- Provide understanding of the techniques essential to the Verilog programming for Verification and Testing.
- To learn the architecture of most prominent vendor in the FPGA market, Xilinx FPGAs and Altera FPGAs.

Course outcome

- Analyze combinational and sequential circuit design concepts.
- Develop FSMs & ASMs for the given problems.
- Write Verilog code, compile, simulate and execute on any VLSI design platform.
- Apply Verilog HDL for FPGA Programming
- Implement Digital Circuits on Xilinx FPGAs and Altera FPGAs using Verilog HDL

Evaluation Systems

Internal Examination	***Component***	***% of Marks***	***Method of Assessment***
	Internal Test I		Written Examination
	Internal Test II		Online (MCQ)
	Assignment		Writtensubmission
	Experiments		Lab Work, Report
	Project		Report and Presentation
	Quiz		Surprise/Preannounced Ones
	Total	*40(T) 50(P/Pj)*	
External Examination	*QA Cell*	*60(T) 50(P/Pj)*	Written Examination

Total		*100*	

Course content

Module I: Design Flow (5 hrs)

Implementation Strategies for Digital ICs: Custom IC Design, Cell-Based Design Methodology. Array Based Implementation Approaches. Traditional And Physical Compiler Based ASIC Flow.

Practice

- EDA Tools : Cadence
- Design Project Organization
- Starting The Design Vision Graphical Environment
- RTL Model Analysis
- Design Elaboration

Module II: RTL Synthesis (5 hrs)

An overview of the synthesis based ASIC design flow. Synthesis Environment. Technology library: technology libraries, logic library basics, delay calculations

Practice

- RTL Design of Pipelined Architecture and Its Performance Evaluation
- Design Constraint Definitions
- Design Mapping and Optimization
- RTL Design of Booth Multiplier Architectures

Module III: Static Time Analysis (7 hrs)

Overview of Timing Verification and Static Timing Analysis. Critical Path. Timing Exceptions. Multi Cycle Paths, False Paths and Timing Constraints (Such As Setup, Hold, Recovery and Pulse Width).

Practice

- Static Timing Analysis of Booth Multiplier

Module IV: Backend Design (8 hrs)

Floor Planning & Place and Route Optimization, Floor planning Styles and Methodology, Global Routing

Practice

- Starting The Encounter Graphical Environment
- Design Import
- Global Net Connections
- Operating Conditions Definition
- Floorplan Specification
- Power Ring/Stripe Creation And Routing
- Core Cell Placement

Module V: Partitioning Style (6 hrs)

Partitioning For Synthesis, Coding Guideline for Synthesis. Logic Inference: Order Dependence. Optimization and Mapping Constraints (Clock, Delay, Area, Design).

Practice

- Design Checks
- Report Generation
- Post-Route Timing Data Extraction
- Post-Route Netlist Generation
- GDSII File Generation

Module VI: Design Methodology for Logic Cores (7 hrs.)

Architecture Of The Present-Day Soc , Design Issues of SoC, Hardwar & Software Design, Core Libraries , EDA Tools SoC Design Flow Guidelines for Design Reuse , Design Process for Soft and Firm Cores , Design Process for Hard Cores, System Integration

Module VII: Design Methodology for Memory & Analog Cores (7 hrs.)

Embedded Memories, Design Methodology for Embedded Memories, Specification of Analog Circuits, Core Level Validation, Core Interface Verification, SoC Design Validation

Practice

- Design of Halftone Image Converter using Cadence

Text Books:

1. Verilog HDL, 2/E By Samir Palnitkar, Pearson Education
2. Himanshu. Bhatnagar, “Advanced ASIC Chip Synthesis” (2/e).KAP.2002
3. Rochit Rajsuman, ‘System-on-a-Chip: Design and Test’, Artech House, 2000

Reference Books:

1. Maheshwari, Naresh, Sapatnekar, "Timing Analysis and Optimization of Sequential Circuits". 1998, Springer. ISBN: 978-0-7923-8321-5
2. Modern Digital Electronics. Author, R P Jain. Edition, 3. Publisher, Tata McGraw-Hill Education

Course outline Prepared by; Dr.Chandra Sekhar Dash and Satyanarayan Padhy
Date:20/05/20

Note: 1 credit theory=10 hrs lecture, 1 credit practice/project=12.5 hrs lab/workshop/field work in a semester

Code	Course Title	T-P-Pj (Credit)	Prerequisite
VLCU2070	Digital VLSI	2-2-0	NIL

Objective

- Focus on understanding of the different CMOS VLSI designs required to carry out a complete digital logic design
- Discuss on design of high speed and low delay VLSI circuits and prepare students for a professional career in the relevant field on completion of degree

Course outcome

- Design any high speed combinational and sequential digital circuit using CMOS logic
- Enhancement of complex digital VLSI logic design skill of students which will help them to complete any project work undertaken in higher semesters
- Pursue a bright career as a VLSI Test Engineer, VHDL Programmer, Embedded design engineer, Software Engineer in the IT sector

Evaluation Systems

Internal Examination	***Component***	***% of Marks***	***Method of Assessment***
	Internal Test I		Written Examination
	Internal Test II		Online (MCQ)
	Assignment		Writtensubmission
	Experiments		Lab Work, Report
	Project		Report and Presentation
	Quiz		Surprise/Preannounced Ones
	Total	*40(T) 50(P)*	
External Examination	*QA Cell*	*60(T) 50(P)*	Written Examination
Total		*100*	

Course content

Module I: Introduction (6 hours)

Issues in Digital IC Design. Quality Metrics of a Digital Design, Manufacturing CMOS Integrated Circuits. Design Rules. Layouts.

Practice

- Layout design of NMOS and PMOS transistor
- Layout design of CMOS inverter
- Study of Full-custom IC Design flow: Schematic simulation, DRC, LVS, QRC, Post Layout Simulation.

Module II: MOS Transistor (6 hours)

The Metal Oxide Semiconductor (MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor (MOSFET), MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effects, MOSFET Capacitance

Practice

- Introduction to EDA tool.
- Study of NMOS and PMOS drain current characteristics and transfer characteristics.
- Extraction of device model parameters.
- Introduction to layout editor and Layout of NMOS and PMOS transistor.

Module III: MOS Inverters (6 hours)

Static CMOS Inverter: Static and Dynamic Behavior Practices of CMOS Inverter. Components of Energy and Power: Switching, Short-Circuit and Leakage Components. Technology scaling and its impact on the inverter metrics.

Practice

- Study of resistive load and enhancement load Inverter static characteristics
- Study of CMOS inverter transfer characteristics.
- Study of variation of VTC curve with different MOS transistor size

Module IV: CMOS Combinational Logic Circuit Design (8 hours)

Static CMOS Design: Complementary CMOS, Ratioed Logic, Pass Transistor Logic. Dynamic CMOS Design: Dynamic Logic Design Considerations. Speed and Power Dissipation of Dynamic logic, Signal integrity issues, Cascading Dynamic gates.

Practice:

- Design and simulation of NAND and NOR gate and study of static characteristics.
- Design and Simulation of complex CMOS logic circuits: half adder, full adder, 2:1 MUX and 4:1 MUX
- Study of NMOS and PMOS pass transistor characteristics.
- Study of transmission gate characteristics.

Module V: CMOS Sequential Logic Circuit Design (8 hours)

Introduction, Bi-stable circuit elements, SR & JK Latch Circuits, Clocked Latch and Flip-Flop Circuits, CMOS D-Latch and Edge-Triggered Flip-Flop.

Practice:

- Design and simulation of latch circuit
- Master-slave edge triggered D flip-flop using multiplexer

Module VI: Semiconductor Memory Design (6 hours)
Introduction, MOS Decoders, SRAM Design, DRAM Design, Memory Architecture and I/O Circuitry

Practice:

- Design and analysis of 6-T conventional SRAM cell
- Design and analysis of DRAM cell

Module VII: Layout Design (Practice) (5 hours)
Layout Basics, Silicon-on Insulator, Berkeley Short Channel IGFET Model, Short Channel Threshold Voltage

Text Books:

1. Sung-Mo Kang and Yusuf Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, Tata McGraw-Hill Publishing Company Limited
2. Jan M,Rabaey, AnanthaChandrakasan, BorivojeNikolic, Digital Integrated Circuits–A Design Perspective, PHI

Reference Books:

1. Wayne Wolf, Modern VLSI Design System – on – Chip Design, PHI

2. K,Eshraghian and N,H,E,Weste, Principles of CMOS VLSI Design – a Systems Perspective, 2nd Edn,, Addison Wesley, 1993

Required Software:

- *Microwind/ Cadence/Tanner Tool*

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Source of reference;Udemy

Note: 1 credit theory=10 hrs lecture, 1 credit practice/project=12.5 hrs lab/workshop/field work in a semester

Code	Course Title	T-P-Pj (Credit)	Prerequisite
VLCU2070	Analog VLSI	2-1-0	NIL

Objective

To design analog IC components and building blocks in CMOS technology. To understand the relationships between devices, circuits and systems. Emphasize the design of practical amplifiers, small systems and their design parameter trade-offs.

Course outcome

- Able to analyze bias circuit using CMOS current mirror.
- Able to design feedback and differential operational amplifier.
- Able to analyze stability of operational amplifiers
- Able to apply frequency compensation techniques for Amplifiers
- Able to analyze basic operation of PLL.

Evaluation Systems

Internal Examination	***Component***	***% of Marks***	***Method of Assessment***
	Internal Test I		Written Examination
	Internal Test II		Online (MCQ)
	Assignment		Written submission
	Experiments		Lab Work, Report
	Project		Report and Presentation
	Quiz		Surprise/Preannounced Ones
	Total	*20(T) 50(P/Pj)*	
External Examination	*QA Cell*	*30(T) 50(P/Pj)*	Written Examination

Total		*100*	

Course content

Module I: MOS Modeling (5 hrs)

MOS Device Models, MOS Current Sources and Sinks, Current Mirror: Basic Current Mirrors, Cascode Current Mirrors. Current and Voltage Reference Circuits**.**

Practice

- Study of VLSI CAD Tools (Working Environment, Introduction to Linux and Vi Editor, Cadence Virtuoso Simulator.

Module II: Amplifier Design (6 hrs)

Basic Concepts of Amplifier, Common Source Stage, Common Gate Stage, Cascode Stage. Differential Stage: Single Ended and Differential Operation. Basic Differential Pair.

Practice

- Design of Single Stage Amplifier.

Module III: Frequency response of Amplifiers (5 hrs)

Miller Effect, Frequency Response of Common Source Stage, Common Gate Stage, Cascode Stage and Differential Pair.

Practice

- Design of Two Stage Amplifier and Frequency Response Analysis.

Module IV: CMOS Op-Amps (6 hrs)

Differential and Common Mode Circuits, Op-Amp CMRR Requirements, Need for Single and Multistage Amplifiers, Effect of Loading in Differential Stage**.**

Practice

- Design of Multi Stage Operational Amplifiers and Study of Loading Effect.

Module V: Stability Analysis (3 hrs)

Stability of Feedback: Basic Concepts, Instability and the Nyquist Criterion, Stability Study for a Frequency-Selective Feedback Network, Root Locus: Effect of Pole Locations on Stability, multipole systems.

Module VI: Frequency Compensation (4 hrs)

Concepts and Techniques for Frequency Compensation – Dominant Pole, Miller Compensation, Compensation of Miller RHP Zero, Nested Miller, Compensation of Two Stage OP-Amps.

Practice

- Determination Poles and Zeros of Amplifier Circuits.

Module VII: Data Converters (4 hrs)

Analog to Digital Converter: Successive Approximation Type, Counter Type, Digital to Analog Converter: Binary Weighted Resistor, R-2R Ladder network.

Text Books:

4. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", McGraw-Hill, 2000.
5. Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", (Second Edition) Oxford University Press, February 2002.

Reference Books:

3. Gray, Hurst, Lewis, and Meyer: "Analysis and design of Analog Integrated Circuits", (4/e), John Wiley and Sons.
4. Gray, Hurst, Lewis, and Meyer: "Analysis and design of Analog Integrated Circuits", (4/e), John Wiley and Sons.

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Date:20/05/20

Note: 1 credit theory=10 hrs lecture, 1 credit practice/project=12.5 hrs lab/workshop/field work in a semester

Code	Course Title	T-P-Pj (Credit)	Prerequisite
CUVL2075	VERIFICATION USING SYSTEM VERILOG & UVM	0-4-0	NIL

Objective

- To Make The Student Understand System Verilog Language And Demonstrate How To Build Verification Environment For Performing Verifications Of VLSI Circuits Using SystemVerilog.

Course outcome

- Students will Be Able to Use Any Simulation or Synthesis Tool that Support SystemVerilog
- Students will Learn How to Take Advantage of The SystemVerilog Language to Make RTL Design ad Synthesis More Productive

Evaluation Systems

Internal Examination	*Component*	*% of Marks*	*Method of Assessment*
	Internal Test I		Written Examination
	Internal Test II		Online (MCQ)
	Assignment		Written submission

	Experiments	*50(P)*	Lab Work, Report
	Project		Report and Presentation
	Quiz		Surprise/Preannounced Ones
	Total	*50(P)*	Practical
External Examination	*QA Cell*	*50(P)*	Practical Examination
Total		*100*	

Course content

Verification Concepts (2 Hrs.)

- Verification Methodologies - Simulation, Formal, Assertions
- Directed Vs Constrained Random Verification - Coverage

Introduction to SystemVerilog Language (6 Hrs.)

- Language Constructs - Data Types and Operators
- Language Constructs - Loops and Control Flows
- Tasks and Functions
- Arrays and Queues

Basic SV TB - Connecting to Design (6 Hrs.)

- Clocking Blocks
- Program Blocks
- Direct Programming Interface (DPI)

SV - OOP Concepts and Randomization (6 Hrs.)

- Basic OOP Concepts
- SystemVerilog Classes Explained
- Virtual Interfaces
- Random Constraints and Usages - Part 1
- Random Constraints - Part 2

Threads and Inter Process Communication (6 Hrs.)

- Processes and Threads in SystemVerilog
- SystemVerilog Mailboxes
- Synchronization - Events and Semaphores

Introduction to Verification Methodologies (14 Hrs.)

- Introduction to Universal Verification Methodology (UVM): Typical UVM Testbench Architecture, UVM Library Class
- UVM Basics: UVM TB Architecture, Creating UVCs and Environment, Creating agent, UVM simulation phases, Test Flow
- Standard Verification Methodologies - Need and evolution
- Introduction to concept of OVM and UVM
- Creating and Using UVM Testbench: Creating UVM Environment: Building a Scoreboard, Building Reusable Environments, Connecting Multiple UVCs

Case Study (12 Hrs.)

- Design and Verification of a SRAM Memory Cell Using UVM Methods

Text Books

1. Sutherland, Stuart, Simon Davidmann, and Peter Flake, "SystemVerilog for Design Second Edition: A Guide to Using System Verilog for Hardware Design and Modeling", Springer Science & Business Media, 2006
2. Spear, Chris. "SystemVerilog for verification: a guide to learning the testbench language features," Springer Science & Business Media, 2008

Reference Books

1. R. Salemi, "The UVM Primer: A Step-By-Step Introduction To The Universal Verification Methodology" Boston Light Press, 2013
2. System Verilog, 3.1a, Language reference manual
3. Vijayaraghavan, Srikanth, and Meyyappan Ramanathan. A practical guide for SystemVerilog assertions. Springer Science & Business Media, 2005
4. Bergeron, J. "Writing Testbenches Using SystemVerilog.—NY: Springer Science and Business Media." (2006)

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Date:20/05/20

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