Chapter 20

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SYSTEM- ON- CHIP

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1. INTRODUCTION

During thinking of a laptop the primary things which come into mind are graphics, processor, I/O, net speed and some more functions. As on today we have different gadgets with much more applications than these. Commendable graphics with AR and VR facility Smartphones are at the doorstep now. There are smartwatches which provide health reports with the help of various sensors. Pocket size computers are available to replace old age laptops.

These smart devices don't have plenty of space. But a PC needs space for a motherboard, RAM, Graphics card, cooling arrangement and others. A system on a chip (SOC) covers all these discrete requirements and places it inside one chip.

The pace of the advancement of the semiconductor industry and the pressure for more composite and concise implementation have driven to a very organized subsequent technology. SIA roadmap predicted billions of transistor and 48 Gbits per chip DRAM density for ASIC applications [1] and it is achieved. With regard to digital design, SOCs are already up to the minute. At present SOCs are primarily obtained by adding various intended cores on the same chip. Design of SOCs faces a lot of challenges which comprises of block to block networking, testing of individuals, power management etc. To develop the rapid growth of semiconductor world this movement of integrating whole system will be more and more nourished and will be made error less.

2. STRUCTURE DESIGN

Reiterating elements, used in other implementation, is a technique to minimize the endeavor. In ASIC design area these reiterating of pieces has been a regular exercise. Because of reduced product cycle and very fast escalating difficulty, a lot of manufacturer prefers outsourcing of cores. Here comes Intellectual property issue. In [2] few key matters for IP restate are figured: standard of sketch, authentication, reliability, reinforce and addition. Figure 1 represents an IP-based structural flow. The stating of new IPs are done on the basis of emerged insistence. Depending on the IP statement a model is introduced. This model can straightway be administered as soft IP.

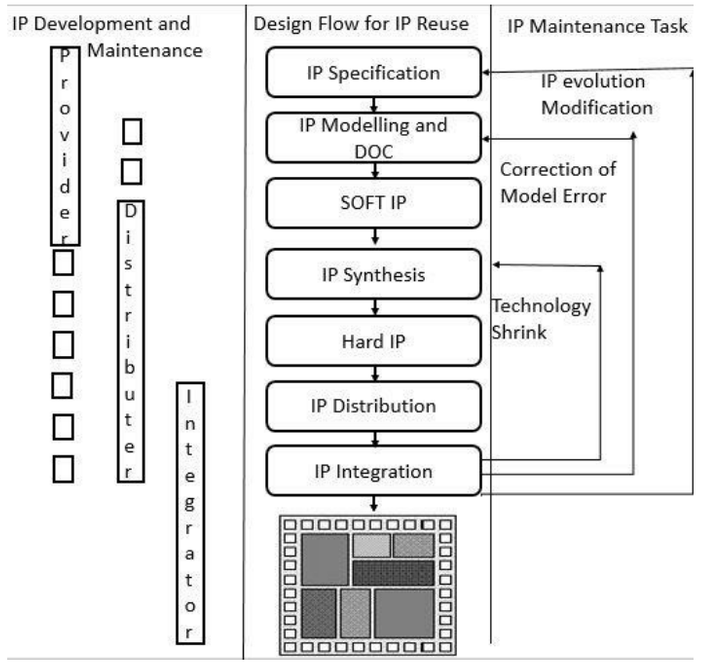

Fig-1 IP Based Structural Flow

The dispersal of the IP can be carried out straightway through the provider. To incorporate the IP block within the user's product development, prop up services need to be furnished. In this diagram, a compact collaboration of the IP provider, distributor and customer is necessary for the sake of improved performance. Although the efficiency of the system is enhanced some short comings are also there: recyclable element in design calls generality. It generally follows by degradation in performance. Additionally continuing technology development demands continuous re-inte-