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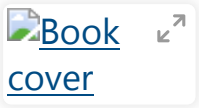

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N-bit Pipelined CSM Based Square Root Circuit for Binary Numbers

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Abstract

Uniqueness is the key to go forward and maintain a spirited advantage in high-end research. By means of interdisciplinary research from the theory of very large-scale integration to signal processing prospective, it provides a systematic approach to the design and analysis of various circuits that are mainly intended for a variety of VLSI signal processing applications. This work presents an efficient design and implementation of n-bit pipelined square root circuit. An idea of a square root circuit with using a controlled subtract-multiplex (CSM) block is introduced here. In this paper, we have implemented a popular algorithm called non-restoring algorithm